202-206

Unit - 1

8

Field Effect Transistors

USO4CELE21

Unit-1

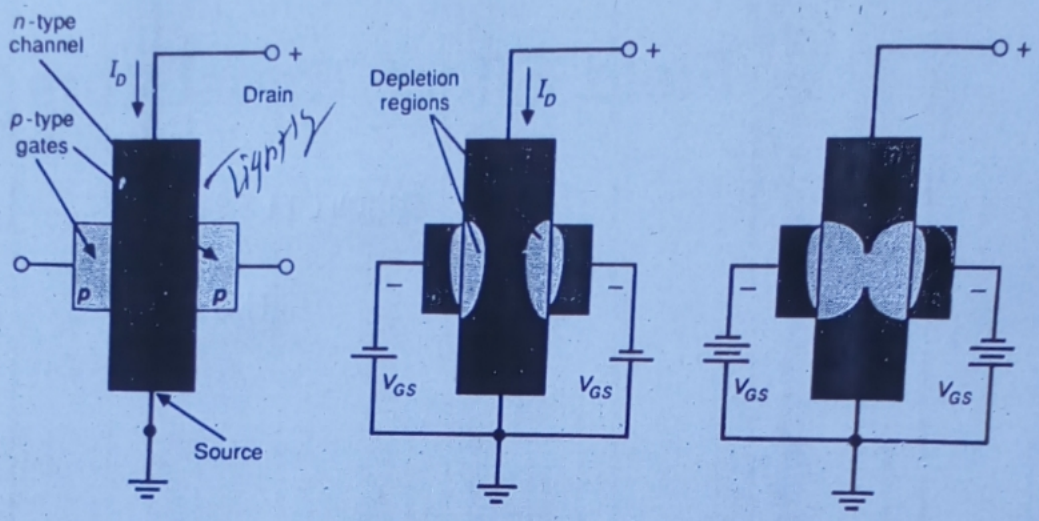
Introduction

The field effect transistor (FET) is a voltage-operated device. Unlike a bipolar transistor, a FET requires virtually no input (signal or bias) current. This gives it an extremely high input resistance, which is its most important advantage over a bipolar transistor. There are two major categories of field effect transistors: junction FETs and MOSFETs. These are further subdivided into *p*-channel and *n*-channel devices. Power MOSFETs, such as the VFET, have superior performance in comparison to bipolar power transistors.

8-1 The *n*-Channel JFET

The operating principle of the *n-channel junction field effect transistor* (JFET) is illustrated by the block representation in Fig. 8-1. A piece of *n*-type material, referred to as the *channel*, has two smaller pieces of *p*-type material attached to its sides, forming *pn*-junctions. The channel's ends are designated the *drain* and the *source*, and the two pieces of *p*-type material are connected together and their terminal is called the *gate*. With the gate terminal not connected, and a potential applied (positive at the drain, negative at the source), a *drain current* I_D flows as shown in Fig. 8-1(a). When the gate is biased negative with respect to the source [Fig. 8-1(b)], the *pn*-junctions are reverse biased and depletion regions are formed. The channel is more lightly doped than the *p*-type gate blocks, so the depletion regions penetrate deeply into the channel. Since a depletion region is a region depleted of charge carriers, it behaves as an insulator. The result is that the channel is narrowed, its resistance is increased, and I_D is reduced. When the negative gate bias voltage is further increased, the depletion regions meet at the center [Fig. 8-1(c)], and I_D is cut off completely.

An ac signal applied to the gate causes the reverse voltage on the junctions to increase as the signal voltage goes negative and decrease as it goes



(a) No bias voltage on gates

(b) Small negative gate-source bias

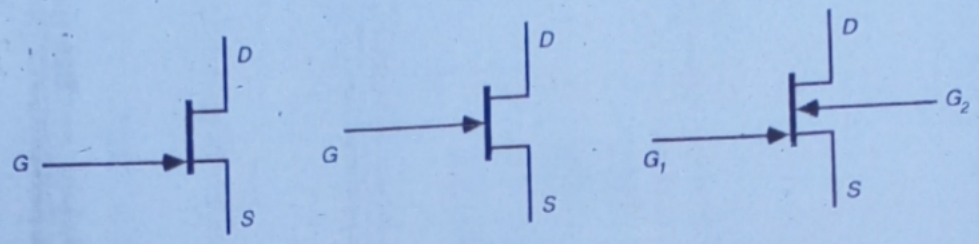
(c) Large negative gate-source bias

Figure 8-1 The *n*-channel JFET consists of an *n*-type channel with two *p*-type gate regions on either side. When the gate-channel junctions are reverse biased, depletion regions penetrate deeply into the channel, thus increasing its resistance.

positive. Consequently, as the signal goes negative, the depletion regions are widened, the channel resistance is increased, and the drain current is reduced. Also, as the signal goes positive, the depletion regions recede, the channel resistance is reduced, and the drain current is increased. As will be seen in Chapter 21, the *n*-channel JFET is comparable to a triode vacuum tube. The drain and source perform the same functions as the plate and cathode, respectively, and, like the grid of a triode, the FET gate controls drain current. As is also the case with a grid, gate current is to be avoided, so the gate–channel junctions are normally never forward biased.

The name *field effect device* comes from the fact that the depletion regions in the channel are the result of the electric field at the reverse-biased gate–channel junctions. The term *unipolar transistor* is sometimes applied to a FET, because unlike a bipolar transistor, the drain current consists of only one type of charge carrier; electrons in the *n*-channel FET and holes in the *p*-channel device (Section 8-3).

The symbol for the *n*-channel JFET is shown in Fig. 8-2. As for other types of transistors, the arrowhead always points from *p* to *n*. For an *n*-channel device, the arrowhead points from the *p*-type gate toward the *n*-type channel.



(a) (b) (c) Tetrode connected

Figure 8-2 Circuit symbols for the *n*-channel JFET. As with all semiconductor symbols, the arrowheads point from *p*-type to *n*-type material.

Some manufacturers use the symbol with the gate terminal opposite the source [Fig. 8-2(a)]; others show the gate centralized between drain and source [Fig. 8-2(b)]. The symbol shown in Fig. 8-2(c) is used where the terminals of the two gate regions are provided with separate connecting leads. In this case the device is referred to as a *tetrode-connected* FET.

8-2 Characteristics of an *n*-Channel JFET

Depletion Regions

An *n*-channel JFET is shown in Fig. 8-3 with the gate connected directly to the source terminal. When a drain voltage V_D is applied, a drain current I_D flows in the direction shown.

Since the *n*-material is resistive, the drain current causes a voltage drop along the channel. In the portion of the channel between gate and source, I_D causes a voltage drop which biases the gate with respect to that part of the channel close to the gate. Thus, in Fig. 8-3, point A is positive with respect to the source. Alternatively, it can be stated that the source terminal is negative with respect to point A. Since the gate regions are connected to the source, the gate regions are negative with respect to point A by a voltage V_A. This will cause the depletion regions to penetrate into the channel at point A by an amount proportional to V_A. Between point B and the source terminal the voltage drop along the channel is V_B, which is less than V_A. Therefore, at point B the gate is at $-V_B$ with respect to the channel, and the depletion region penetration is less than that at point A. From point C to the source terminal, the voltage drop V_C is less than V_B. Thus, the gate–channel junction reverse bias (at point C) is V_C volts, and penetration by the depletion regions is less than at A or B. This difference in voltage drops along the channel, together with the consequent variation in bias, accounts for the shape of the depletion regions penetrating the *n*-channel.

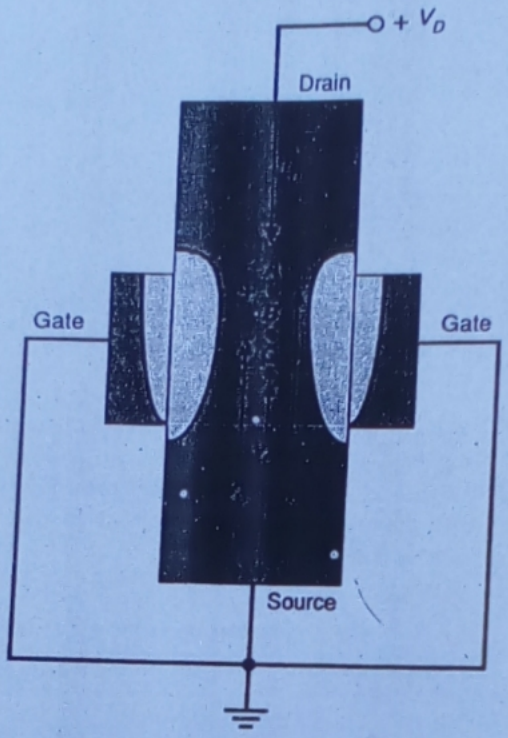
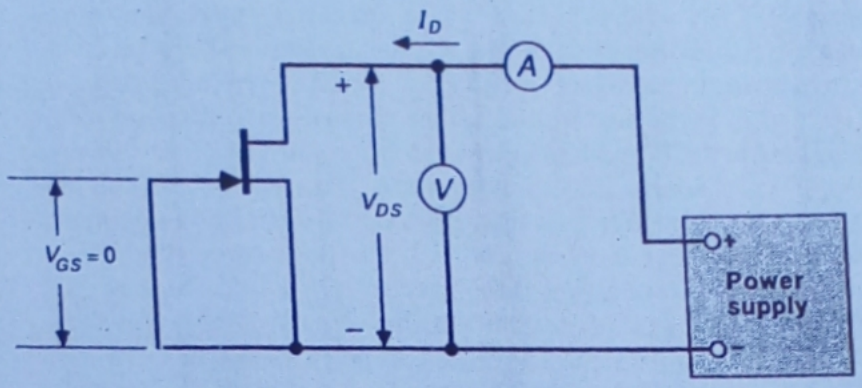


Figure 8-3 Drain current flowing in an *n*-channel JFET causes voltages drops along the channel. The voltage drop from point *A* to the source is greater than that from point *B* to the source. This makes the gates more negative with respect to point *A* than with respect to point *B* and results in greatest depletion region penetration at point *A*.

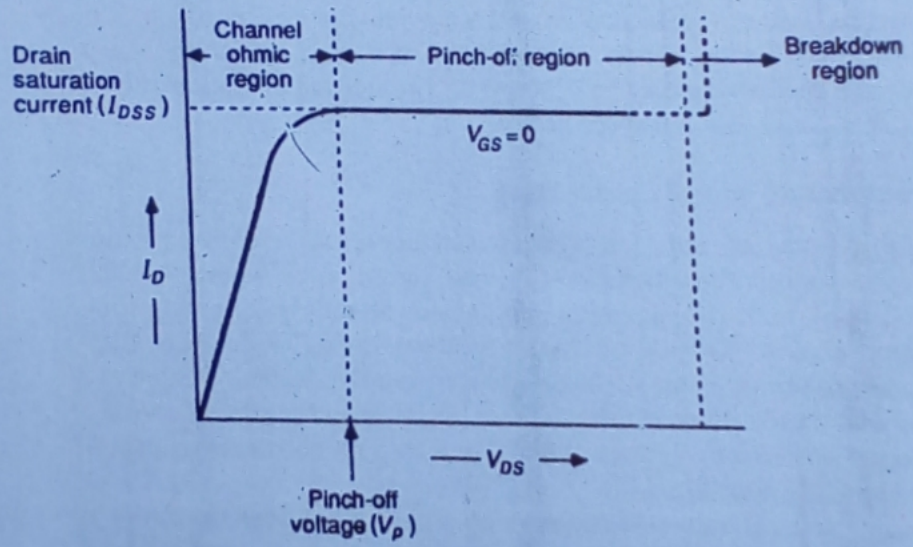
Drain Characteristics when $V_{GS}=0$

The circuit in Fig. 8-4(a) shows the FET gate connected directly to the source, giving $V_{GS} = 0$. The drain characteristic for $V_{GS} = 0$ is plotted from the corresponding I_D and V_{DS} levels measured as V_{DS} is increased from zero.

The drain characteristic for $V_{GS} = 0$ is plotted in Fig. 8-4(b). When $V_{DS} = 0$, $I_D = 0$, and the voltage between the gate and all points in the channel is also equal to zero. When V_{DS} is increased by a small amount, a small drain current flows, causing some voltage drop along the channel. This reverse biases the gate–channel junctions by a small amount, causing little depletion region penetration and having negligible effect on the channel resistance. With further small increases in V_{DS} the drain current increase is nearly linear, and the channel behaves as a resistance of almost constant value.



(a) Circuit for obtaining FET drain characteristic when $V_{GS} = 0$



(b) FET drain characteristic for $V_{GS} = 0$

Figure 8-4 Drain characteristics for an *n*-channel JFET with $V_{GS} = 0$. When the drain–source voltage V_{DS} is increased from zero, the FET initially behaves as a constant-value resistance. At the higher levels of drain current, depletion region penetration limits the current flow to an almost constant level.

The channel continues to behave as an almost constant resistance, until the voltage drop along it becomes large enough to cause considerable penetration by the depletion regions. At this stage the channel resistance is significantly affected by the depletion regions. Further increases in V_{DS} produce

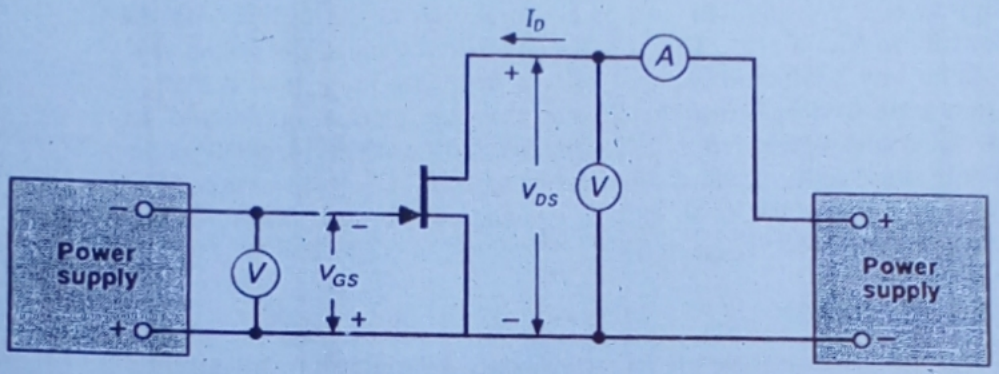
smaller increases in I_D, which, in turn, cause increased penetration by the depletion regions and further increase the channel resistance. Because of the rapid increase in channel resistance at this stage (produced by increasing I_D), a *saturation level* of I_D is reached where further increases in V_{DS} produce only very slight increases in I_D. The drain current at this point, with V_{GS} at zero, is referred to as the *drain–source saturation current* I_{DSS} (see Fig. 8-4). When the drain current saturation level is reached, the shape of the depletion regions is such that they appear to *pinch off* the channel. For this reason, the drain–source voltage at which I_D levels off is designated the *pinch-off voltage* V_P, as indicated in Fig. 8-4. The region of the characteristic where I_D is fairly constant is referred to as the *pinch-off region*. The region of the characteristic between $V_{DS} = 0$ and $V_{DS} = V_P$ is termed the *channel ohmic region*, because the channel is behaving as a resistance. With continued increase in V_{DS}, a voltage will be reached at which the gate–channel junction breaks down. This is the result of the charge carriers which make up the reverse saturation current at the gate channel junction being accelerated to a highly velocity and producing an *avalanche effect* (see Section 16-2). At this point the drain current increases very rapidly, and the device may be destroyed. The normal operating region of the characteristics is the pinch-off region.

Drain Characteristics with External Bias

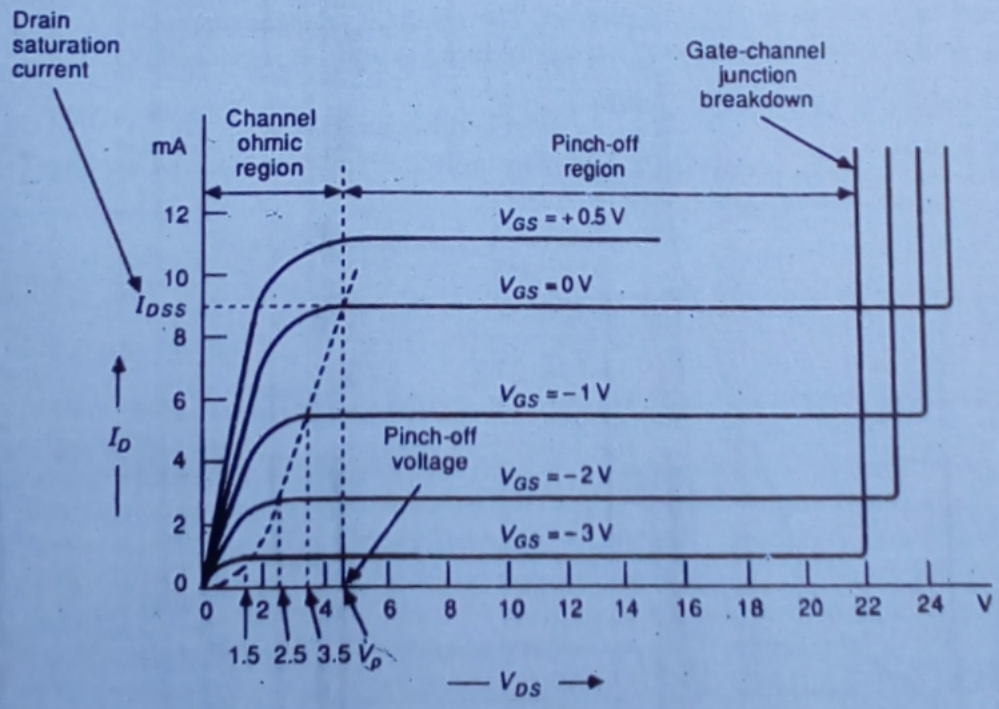
When an external bias of, say, −1 V is applied between the gate and the source, the gate–channel junctions are reverse biased even when $I_D = 0$. Therefore, when $V_{DS} = 0$, the depletion regions are already penetrating the channel to some extent. Because of this, a smaller voltage drop along the channel (i.e., smaller than when $V_{GS} = 0$) will increase the depletion regions to the point at which they pinch off the current. Consequently, the pinch-off voltage is reached at a lower I_D than when $V_{GS} = 0$. The characteristic for $V_{GS} = -1$ V is shown in Fig. 8-5.

By employing several values of negative external bias voltage, a family of drain characteristics is obtained as shown in Fig. 8-5(b). Note that the value of V_{DS} for breakdown is reduced as the negative gate bias voltage is increased. This is because $-V_{GS}$ is adding to the reverse bias at the junction. If a positive gate bias voltage is employed, a larger I_D can be the result, as shown by the characteristic for $V_{GS} = +0.5$ V. In general, however, V_{GS} is maintained negative to avoid the possibility of forward biasing the gate–channel junctions.

The broken line on Fig. 8-5(b) is a line through the points at which I_D saturates for each level of gate bias voltage. When $V_{GS} = 0$, I_D saturates at I_{DSS}, and the characteristic shows $V_P = 4.5$ V. When an external bias of −1 V is applied, the gate–channel junctions still require −4.5 V to achieve pinch-off. This means that a 3.5 V drop is now required along the channel instead of the previous 4.5 V, and the 3.5 V drop is achieved with a lower value of I_D. Similarly, when V_{GS} is −2 V and −3 V, pinch-off is achieved with 2.5 V and



(a) Circuit for obtaining FET drain characteristics



(b) Family of FET drain characteristics for various levels of gate-source bias voltage

Figure 8-5 Circuit for obtaining FET drain characteristics and family of drain characteristics for an *n*-channel JFET. When gate–source bias voltage V_{GS} is −1 V, −2 V, etc., drain current I_D saturates at progressively lower levels.

1.5 V, respectively, along the channel. The 2.5 and 1.5 V drops are, of course, achieved with further reduced values of I_D.

Suppose 4.5 V is applied as a gate–source bias to the device with the characteristics in Fig. 8-5(b). This is a V_{GS} equal to the pinch-off voltage V_P. Now, without any additional channel voltage drop due to I_D, the depletion regions penetrate so deeply into the channel that they meet at the middle. In this case, I_D is completely cut off. So the pinch-off voltage, applied as an external gate bias, reduces the drain current to zero. The gate–source bias voltage required to reduce I_D to zero is designated the *gate cutoff voltage* $V_{GS(off)}$, and, as explained, $V_{GS(off)} = V_P$.

Transfer Characteristics

The FET *transfer characteristics* are experimentally determined using the circuit of Fig. 8-5(a). Drain–source voltage V_{DS} is maintained at a constant level, and V_{GS} is adjusted in convenient steps. At each step of V_{GS}, the I_D and corresponding V_{GS} levels are recorded. Thus, a table of values is obtained from which a graph of I_D versus V_{GS} may be plotted. The resultant transfer characteristic (Fig. 8-6) shows that I_D is progressively reduced as $-V_{GS}$ is increased,

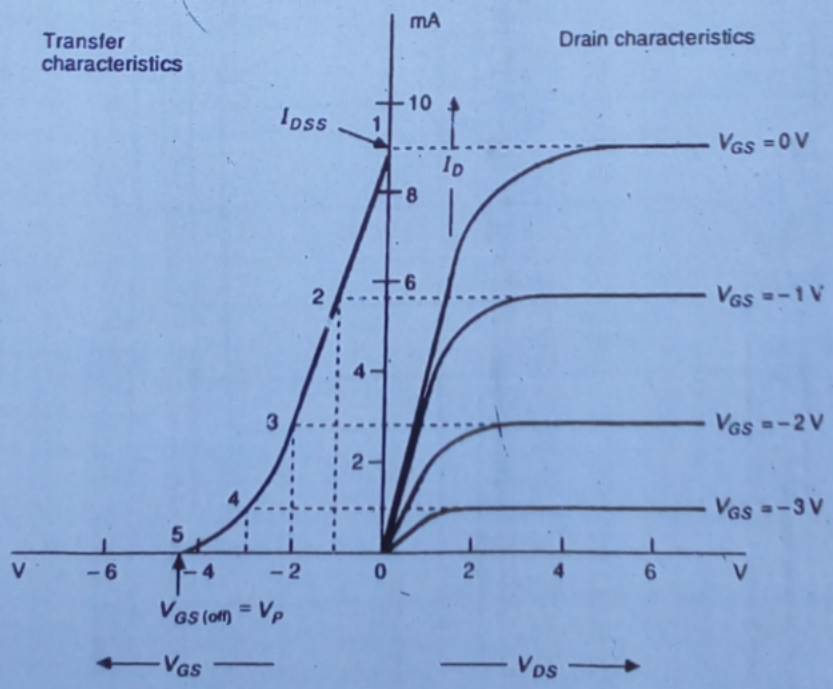


Figure 8-6 Derivation of transfer characteristics from drain characteristics. The transfer characteristics show the relationship between I_D and V_{GS} when V_{DS} is a constant quantity.

and that, as already explained, I_D goes to zero when the reverse gate–source bias voltage is $V_{GS(off)} = V_P$.

As in the case of other devices, the transfer characteristic may be derived from the drain characteristics (see Fig. 8-6). For a constant V_{DS} level, corresponding V_{GS} and I_D values are noted and used to plot the graph of I_D versus V_{GS}.

Example 8-1

Derive the transfer characteristics from the FET drain characteristics in Fig. 8-6.

Solution

Refer to the drain characteristics in Fig. 8-6; when $V_{GS} = 0$, $I_D = 9$ mA. Mark point 1 on the transfer characteristics at $I_D = 9$ mA and $V_{GS} = 0$.

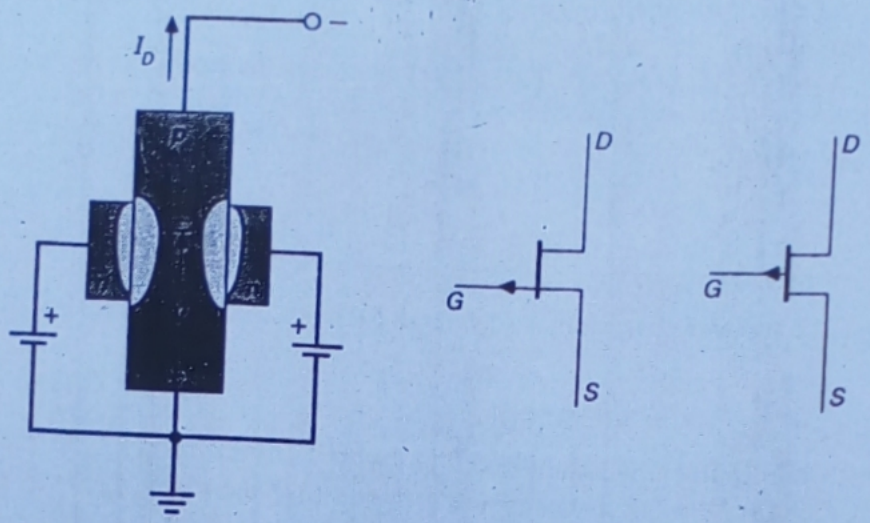
Point 2 is at $I_D = 5.4$ mA and $V_{GS} = -1$ V
Point 3 is at $I_D = 2.8$ mA and $V_{GS} = -2$ V
Point 4 is at $I_D = 0.9$ mA and $V_{GS} = -3$ V
Point 5 is at $I_D = 0$ mA and $V_{GS} = V_P = -4.5$ V

Draw the transfer characteristics through points 1 to 5.

8-3 The p-Channel JFET

In the *p*-channel JFET, the channel is *p*-type material and the gate regions are *n*-type [Fig. 8-7(a)]. The drain–source potential is applied positive to the source and negative to the drain. Thus, a current flows (in the conventional direction) from the source to the drain. To reverse bias the junctions between the gate and the channel, the *n*-type gate must be made positive with respect to the *p*-type channel. Therefore, bias voltage is applied positive on the gate and negative on the source. The voltage drop along the channel is negative at the depletion regions and positive at the source, as illustrated. As in the case of the *n*-channel device, the channel voltage drop tends to reverse bias the gate–channel junctions.

Symbols for the *p*-channel JFET are shown in Fig. 8-7(b). The arrowhead again points from the *p*-type material to the *n*-type material; in this case it points from the *p*-type channel to the *n*-type gate. The drain and transconductance characteristics for the *p*-channel JFET are similar to those of an *n*-channel device, except that all voltage and current polarities are inverted (Fig. 8-8).



(a) p-channel FET

(b) Circuit symbols for p-channel FET

Figure 8-7 The p-channel JFET operates in exactly the same way as an n-channel device, except that the current direction and voltage polarities are reversed. In the graphic symbol for a p-channel device, the arrowhead points from the p-type channel to the n-type gate.

8-4 JFET Data Sheet and Parameters

Data Sheet

A typical FET data sheet is shown in Appendix 1-8, and a portion of it is reproduced in Fig. 8-9. Like the bipolar transistor data sheet, it begins with a device type number and a brief description of the device to indicate the most important applications. These data are followed by the maximum ratings for the FET, and then the electrical characteristics are noted for specified bias conditions. Some of the important FET parameters listed on the data sheet are considered below.

Saturation Current and Pinch-off Voltage

The *drain–source saturation current* I_{DSS} and the *pinch-off voltage* V_P have already been discussed in Section 8-2. I_{DSS} is sometimes termed the *pinch-off current* and is referred to as I_{DP} at $V_{GS} = 0$. I_{DP} may also be specified at values of V_{GS} other than zero, and in this case V_{GS} will also be specified.

The FET transfer characteristic approximately follows the equation

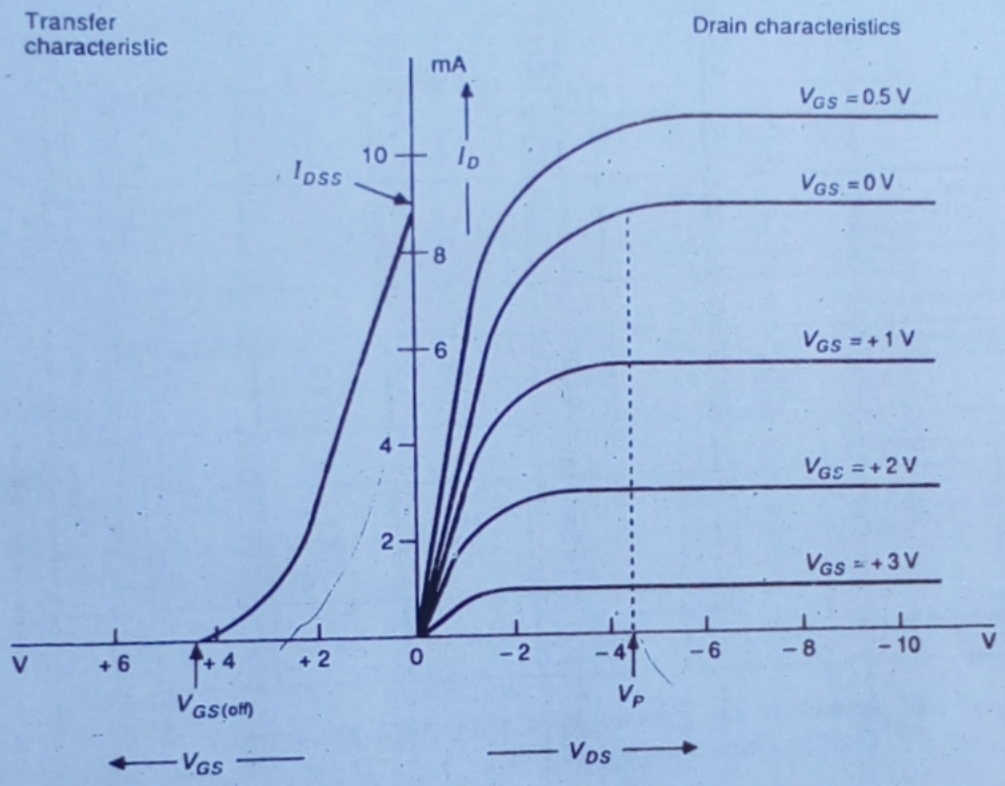


Figure 8-8 Drain and transfer characteristics for a *p*-channel FET. Progressively more positive levels of V_{GS} are required to reduce I_D from its level at $V_{GS} = 0$.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \qquad (8\text{-}1)$$

When I_{DSS} and V_P are known, a table of values of I_D and V_{GS} may be determined from Eq. 8-1. From this table, the transfer characteristic can be constructed. One of the problems in using FETs is that the transfer characteristics can differ substantially from one device to another, even with FETs having the same type number. This is because I_{DSS} and V_P cannot be specified precisely. Instead, the manufacturer specifies maximum and minimum values for each parameter. Referring to Fig. 8-9, it is seen that, for the 2N5457 FET, $I_{DSS(min)} = 1$ mA and $I_{DSS(max)} = 5$ mA. Also, V_P, which is listed as $V_{GS(off)}$, has a minimum level of 0.5 V and a maximum of 6 V.

Example 8-2

Using the information provided on the data sheet (Fig. 8-9), construct the maximum and minimum transfer characteristic for a 2N5459 FET.

			Min	Typ	Max	
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	2N5457 2N5458 2N5459	$V_{GS(off)}$	0.5 1.0 2.0	— — —	6.0 7.0 8.0	Vdc
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 100 μAdc) (V_{DS} = 15 Vdc, I_D = 200 μAdc) (V_{DS} = 15 Vdc, I_D = 400 μAdc)	2N5457 2N5458 2N5459	V_{GS}	— — —	2.5 3.5 4.5	— — —	Vdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current (1) (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5457 2N5458 2N5459	I_{DSS}	1.0 2.0 4.0	3.0 6.0 9.0	5.0 9.0 16	mAdc
DYNAMIC CHARACTERISTICS						
Forward Transfer Admittance (1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 kHz)	2N5457 2N5458 2N5459	$\lvert y_{fs} \rvert$	1000 1500 2000	3000 4000 4500	5000 5500 6000	μmhos
Output Admittance (1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 kHz)		$\lvert y_{os} \rvert$	—	10	50	μmhos

Figure 8-9 Portion of the manufacturer's data sheet for 2N5457, 2N5458, and 2N5459 silicon *n*-channel JFETs.

Solution

From Fig. 8-9,

$$V_P = V_{GS(off)} = 2 \text{ V (min)}, 8 \text{ V (max)}$$
$$I_{DSS} = 4 \text{ mA (min)}, 16 \text{ mA (max)}$$

To construct the minimum transfer characteristic, the minimum levels of V_P and I_{DSS} are substituted into Eq. 8-1 along with convenient values of V_{GS}. Thus, when $V_{GS} = 0$ V,

$$I_D = 4 \text{ mA } [1 - 0/2]^2 = 4 \text{ mA}$$

Accordingly, plot point 1 of the minimum transfer characteristic at $V_{GS} = 0$ V and $I_D = 4$ mA (Fig. 8-10).

When $V_{GS} = 0.5$ V, $I_D = 4 \text{ mA } [1 - 0.5/2]^2 = 2.25 \text{ mA}$ (point 2)
When $V_{GS} = 1$ V, $I_D = 4 \text{ mA } [1 - 1/2]^2 = 1 \text{ mA}$ (point 3)
When $V_{GS} = 1.5$ V, $I_D = 4 \text{ mA } [1 - 1.5/2]^2 = 0.25 \text{ mA}$ (point 4)
When $V_{GS} = 2$ V, $I_D = 4 \text{ mA } [1 - 2/2]^2 = 0 \text{ mA}$ (point 5)

The minimum transfer characteristic is now drawn through points 1 to 5. For the maximum transfer characteristic, the above process is repeated using $I_{DSS} = 16$ mA and $V_P = 8$ V:

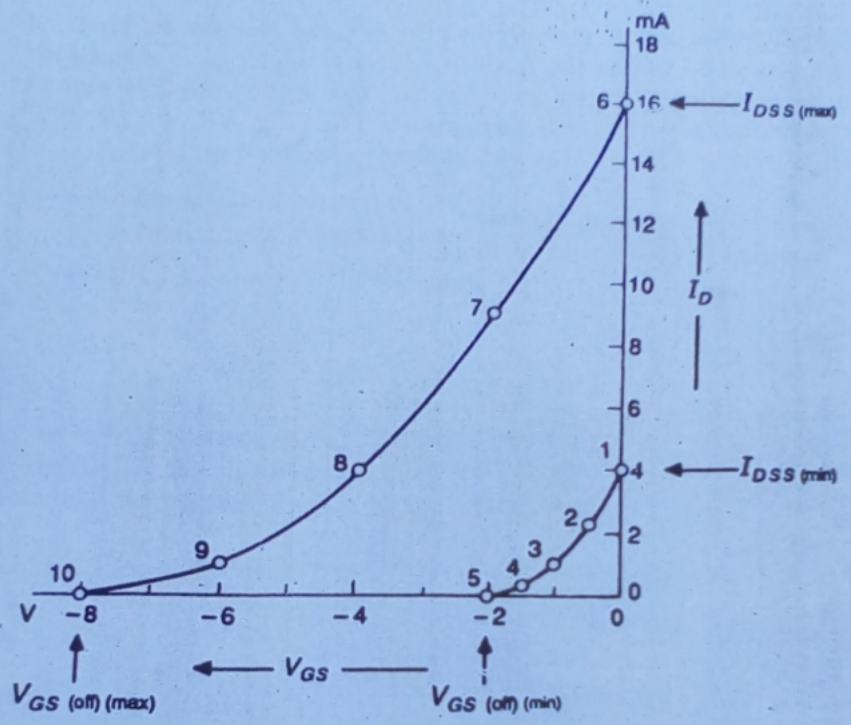


Figure 8-10 Maximum and minimum transfer characteristics for 2N5459, constructed from the data sheet parameters and Eq. 8-1.

When $V_{GS} = 0$ V, $I_D = 16\ \text{mA}\ [1 - 0/8]^2 = 16$ mA (point 6)
When $V_{GS} = 2$ V, $I_D = 9$ mA (point 7)
When $V_{GS} = 4$ V, $I_D = 4$ mA (point 8)
When $V_{GS} = 6$ V, $I_D = 1$ mA (point 9)
When $V_{GS} = 8$ V, $I_D = 0$ mA (point 10)

The maximum transfer characteristic is now drawn through the points as plotted.

Transconductance

It has been shown that I_{DSS} and V_P can be determined from the drain and transfer characteristics. The *transconductance* g_m is another quantity that can be determined from the characteristics. The transconductance defines how the drain current varies in relation to the gate–source voltage. Units of g_m are microsiemens (μS), or microamps per volt (μA / V). Millisiemens (mS), or milliamps per volt (mA / V), may also be used. In a FET with a g_m of 2 mA / V, I_D changes by 2 mA when V_{GS} is altered by 1 V.

Transconductance can be measured as the slope of the transfer characteristic. Since the slope varies, the I_D or V_{GS} level at which g_m is measured should also be specified. *Forward transfer admittance* and *transadmittance* (Y_{fs}), are other names given to transconductance. From Fig. 8-9, the 2N5457 typically has $g_m = Y_{fs} = 300\ \mu S$. Transconductance is defined as:

$$g_m = \frac{\text{variation in drain current}}{\text{variation in gate–source voltage}} \quad \begin{cases}\text{when the drain–source}\\ \text{voltage is maintained}\\ \text{constant}\end{cases}$$

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}} \tag{8-2}$$

Example 8-3 From the FET maximum transfer characteristics given in Fig. 8-11, determine g_m at $V_{GS} = -1$ V and $V_{GS} = -4$ V.

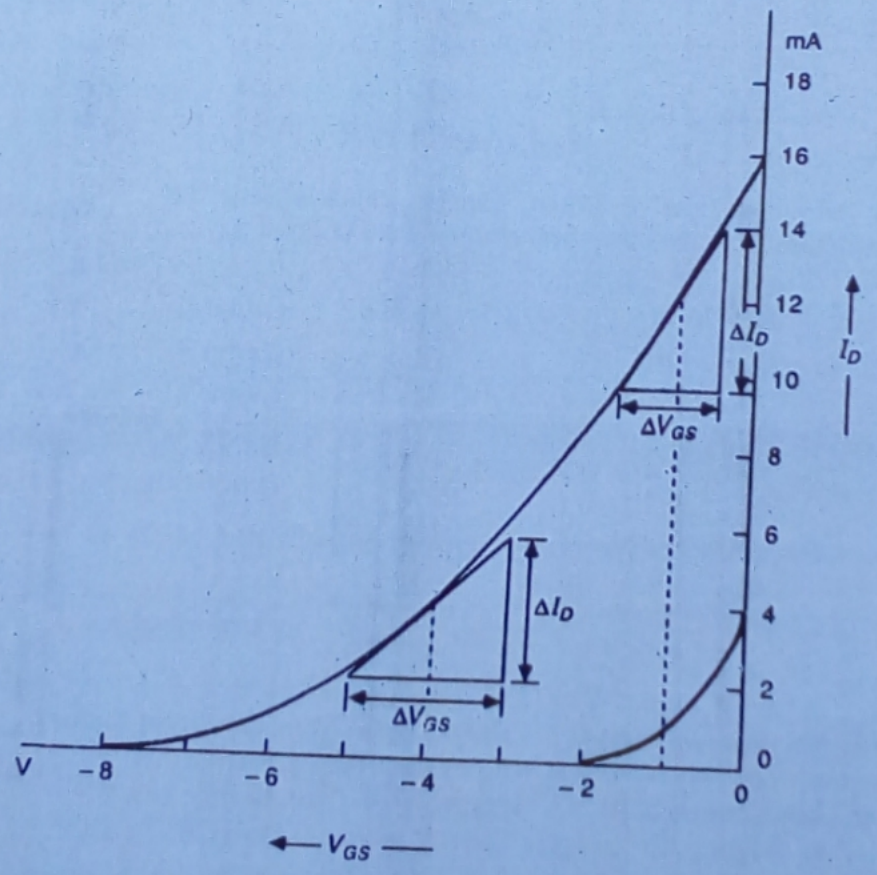


Figure 8-11 The transconductance g_m for a FET can be measured as the slope of the transfer characteristic.

Solution

From Fig. 8-11 and Eq. 8-2,

$$\text{at } V_{GS} = -1 \text{ V}, \quad g_m = \frac{4.3 \text{ mA}}{1.25 \text{ V}} = 3.4 \text{ mA/V} = 3400 \ \mu\text{S}$$

$$\text{at } V_{GS} = -4 \text{ V}, \quad g_m = \frac{3.8 \text{ mA}}{2 \text{ V}} = 1.9 \text{ mA/V} = 1900 \ \mu\text{S}$$

Since the FET transfer characteristic is defined by Eq. 8-1, an equation relating g_m and V_{GS} can be derived by differentiating Eq. 8-1:

$$g_m = \frac{2I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right] \tag{8-3}$$

Using Eq. (8-3), the value of g_m may be calculated for any given level of V_{GS}. As in Eq. (8-1), the negative sign for V_{GS} is already included in the equation, so that only the numerical value of V_{GS} should be entered.

Example 8-4

For the maximum transfer characteristic in Fig. 8-11, use Eq. 8-3 to calculate g_m at $V_{GS} = -1$ V and at $V_{GS} = -4$ V.

Solution

Eq. 8-3,
$$g_m = \frac{2I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right]$$

At $V_{GS} = -1$ V,

$$g_m = \frac{2 \times 16 \text{ mA}}{8 \text{ V}}\left[1 - \frac{1 \text{ V}}{8 \text{ V}}\right]$$
$$= 3500 \ \mu\text{S}$$

At $V_{GS} = -4$ V,

$$g_m = \frac{2 \times 16 \text{ mA}}{8 \text{ V}}\left[1 - \frac{4 \text{ V}}{8 \text{ V}}\right]$$
$$= 2000 \ \mu\text{S}$$

These results are comparable to those obtained directly from the characteristics in Example 8-3.

Drain Resistance

The drain resistance r_d is the ac resistance between drain and source terminals when the FET is operating in the pinch-off region. It is also the slope of the

drain characteristics in the pinch-off region. Since the characteristics are almost flat (Fig. 8-5), r_d is not easily determined from the characteristics. r_d may also be designated as r_{DSS}, and in either case the units are ohms, kilohms, or megohms. Since r_d is usually the output resistance of the FET, it may also be expressed as an *output admittance*: $|Y_{os}| = 1/r_d$.

Drain resistance is defined as

$$r_d = \frac{\text{variation in drain–source voltage}}{\text{variation in drain current}} \begin{cases} \text{when the gate–} \\ \text{source voltage is} \\ \text{maintained constant} \end{cases}$$

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}} \tag{8-4}$$

From Fig. 8-9, $|Y_{os}|$ is 10 μS typically and 50 μS at maximum. This corresponds to r_d = 100 kΩ typically and 20 kΩ minimum.

Drain–Source ON Resistance

The drain resistance r_d is not to be confused with the *drain–source ON resistance* R_{DS}, also designated $R_{D(on)}$. Whereas r_d is a dynamic (or ac) quantity, R_{DS} is the dc resistance of the channel when the depletion regions are absent, i.e., when the device is biased *on* in the channel ohmic region of the characteristics. $I_D \times R_{DS}$ gives a *drain–source ON voltage* $V_{DS(on)}$ which is similar to the $V_{CE(sat)}$ of bipolar transistors. R_{DS} may be typically 100 Ω or much less, and it is an important quantity for FETs used in switching circuits known as *sampling gates*. $I_D \times R_{DS}$ can be much smaller than $V_{CE(sat)}$, making the FET sampling gate superior to the bipolar transistor sampling gates.

Gate Cutoff Current and Input Resistance

The gate–channel junction in a JFET is a *pn*-junction, and since it is normally reverse biased, a minority charge carrier current flows. This is the *gate–source cutoff current* I_{GSS}, also called the *gate reverse current*. For the 2N5457, I_{GSS} = 1 nA at 25°C and 200 nA at 100°C (Appendix 1-8). The device *input resistance* R_{GS} is the resistance of the reverse-biased gate–channel junctions and is inversely proportional to I_{GSS}. Typical values of R_{GS} for a JFET are 10^9 Ω at 25°C and 10^7 Ω at 100°C.

Breakdown Voltage

There are several ways in which the FET breakdown voltage may be specified. BV_{DGO} is the *drain–gate breakdown voltage* with the source open-circuited. BV_{GSS} is the *gate–source breakdown voltage* with the drain shorted to the source. Typical values for each are in the region of 25 V; see the 2N5457 data sheet in Appendix 1-8. Both are a measure of the voltage at which the reverse-biased gate–channel junctions break down.

Noise Figure

One advantage of a FET over a bipolar transistor is that the FET usually has much lower thermal noise. This is because, unlike the bipolar transistor, there are very few charge carriers crossing a junction in the FET. As in the case of bipolar device, the FET *noise figure NF* is specified as a *spot noise figure* at a particular frequency and bias conditions, and for a given value of bias resistance. The figure varies if any of these conditions are altered. Noise calculations for a FET circuit are performed in the same way as for a bipolar transistor circuit.

Capacitances

Capacitances for FETs may be specified as *gate–drain capacitance* C_{gd}, *gate–source capacitance* C_{gs}, and *drain–source capacitance* C_{ds}. Instead of these, the capacitance is sometimes specified as the *common source input capacitance* C_{iss} or C_{gss}. This is the gate–source capacitance measured with the drain shorted to the source. In this case a *reverse transfer capacitance* C_{rss} is also specified, C_{rss} being another term for C_{gd}. These quantities are very important for FET high-frequency and switching circuits. For the 2N5457, C_{iss} is 7 pF maximum and C_{rss} is 3 pF maximum (Appendix 1-8).

8-5 FET Voltage Amplification

As already explained, the FET is a voltage-operated device. A change in gate–source voltage V_{GS} produces a change in drain current I_D. The change in I_D results in a change in output voltage V_D.

Consider the basic FET circuit shown in Fig. 8-12. Note that the gate–source is reverse biased by dc voltage V_G. A signal generator voltage V_i is included in series with the device gate. The drain is supplied by dc voltage V_{DD}.

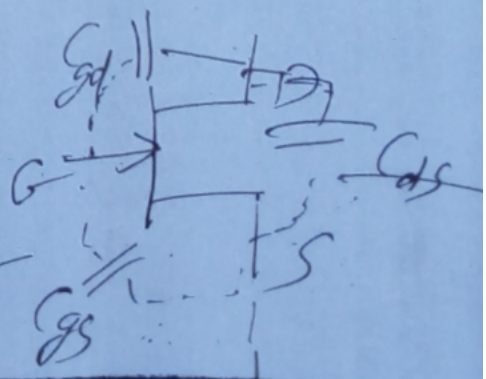
Suppose that $V_{DD} = 20$ V, $R_1 = 6$ kΩ, $g_m = 2000$ μS, and V_G is adjusted to give $I_D = 2$ mA. Then, when $V_i = 0$,

$$\begin{aligned} V_D &= V_{DD} - I_D R_1 \\ &= 20 \text{ V} - (2 \text{ mA} \times 6 \text{ k}\Omega) \\ &= 8 \text{ V} \end{aligned}$$

Now assume that the signal generator voltage is increased from zero to $v_i = \pm 50$ mV. This produces a change in I_D given by

$$\begin{aligned} \Delta I_D &= g_m V_i \\ &= 2000 \text{ μS} \times (\pm 50 \text{ mV}) \\ &= \pm 0.1 \text{ mA} \end{aligned}$$

When $\Delta I_D = +0.1$ mA,



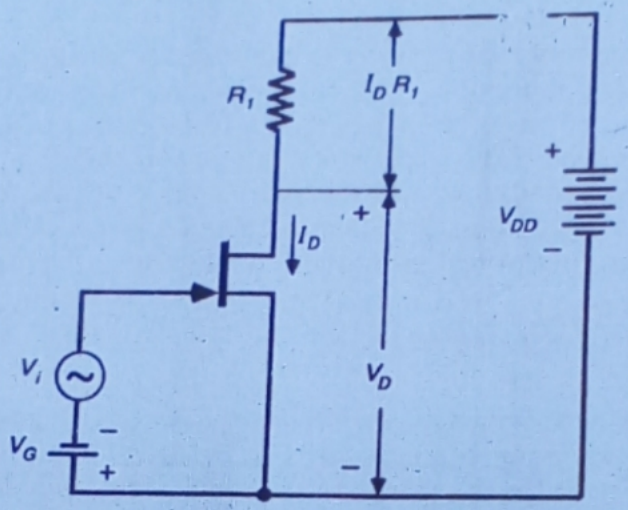


Figure 8-12 When a signal voltage $\pm V_i$ is applied to the gate of a FET, it produces a change in drain current $\pm \Delta I_D$. This change, in turn, alters the voltage drop across R_1, to give a change in (output) drain voltage $\pm \Delta V_D$.

$$\begin{aligned} V_D &= V_{DD} - R_1(I_D + \Delta I_D) \\ &= 20 \text{ V} - 6 \text{ k}\Omega \text{ (2 mA + 0.1 mA)} \\ &= 7.4 \text{ V} \end{aligned}$$

Thus, V_D has fallen from 8 V to 7.4 V, or

$$\Delta V_D = -0.6 \text{ V}$$

When $\Delta I_D = -0.1$ mA,

$$\begin{aligned} V_D &= 20 \text{ V} - 6 \text{ k}\Omega(2 \text{ mA} - 0.1 \text{ mA}) \\ &= 8.6 \text{ V} \end{aligned}$$

Hence, V_D has increased from 8 V to 8.6 V, or

$$\Delta V_D = +0.6 \text{ V}$$

It is seen, then, that a signal of $v_i = \pm 50$ mV produced an output of $v_o = \pm 0.6$ V. The voltage amplification is

$$\begin{aligned} A_v &= \frac{v_o}{v_i} \\ &= \frac{\pm 0.6 \text{ V}}{\pm 50 \text{ mV}} \\ &= 12 \end{aligned}$$

$$Q = V_{CE} \times I_C$$
$$= 25\ \text{V} \times 1\ \text{A} = 25\ \text{W}$$

The case-to-air thermal impedance is

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

From Eq. 7-1,

$$\theta_{CS} + \theta_{SA} = \frac{T_J - T_A}{Q} - \theta_{JC}$$
$$= \frac{90°\text{C} - 25°\text{C}}{25\ \text{W}} - 1°\text{C/W} = 1.6°\text{C/W}$$

From Appendix 1-7, the NC-421, NC-423, and NC-441 all have θ_{CA} less than 1.6°C/W. Choose the smalier and least expensive of the three—the NC-421.

7-4 Decibels and Frequency Response

Decibels

When the output power of an amplifier changes from P_1 to P_2, the power change is expressed as the log of their ratio:

$$\text{Power change} = \log_{10}\left(\frac{P_2}{P_1}\right)\text{(bels)}$$
$$= 10 \log_{10}\left(\frac{P_2}{P_1}\right)\text{decibels (dB)} \qquad (7\text{-}2)$$

Thus, the decibel is a unit of relative power *change*.

The output power dissipated in a load resistance is

$$P_o = \frac{V_o^2}{R_L}$$

So
$$\text{power change} = 10 \log_{10}\left[\frac{V_2^2 R_L}{V_1^2 / R_L}\right]\text{dB}$$
$$= 10 \log_{10}\left[\frac{V_2}{V_1}\right]^2\text{dB}$$
$$= 20 \log\left[\frac{V_2}{V_1}\right]\text{dB} \qquad (7\text{-}3)$$

Also,
$$P_o = I_o^2 R_L$$

So
$$\text{power change} = 10 \log_{10}\left[\frac{I_2^2 R_L}{I_1^2 R_L}\right]\text{dB}$$

$$= 20 \log_{10}\left[\frac{I_2}{I_1}\right] \text{dB} \qquad (7\text{-}4)$$

By means of Eqs. (7-3) and (7-4), power changes can be calculated in decibels using either voltage ratios or current ratios.

Example 7-4

The output power from an amplifier is 50 mW when the signal frequency is 5 kHz. When the frequency is increased to 20 kHz, the output power falls to 25 mW. Calculate the decibel change in output power.

Solution

From Eq. 7-2,

$$\text{power change} = 10 \log_{10}\left[\frac{P_2}{P_1}\right] \text{dB}$$

$$= 10 \log_{10}\left[\frac{25 \text{ mW}}{50 \text{ mW}}\right]$$

$$= -3 \text{ dB}$$

Example 7-5

The output voltage of an amplifier is measured as 1 V at 5 kHz and 0.707 V at 20 kHz. Calculate the decibel change in output power.

Solution

From Eq. 7-3,

$$\text{power change} = 20 \log_{10}\left[\frac{V_2}{V_1}\right] \text{dB}$$

$$= 20 \log_{10}\left[\frac{0.707}{1}\right]$$

$$= -3 \text{ dB}$$

It is seen from Examples 7-4 and 7-5 that the output power of an amplifier is reduced by 3 dB when the measured power falls to half its normal level, or when the measured voltage falls to 0.707 of its normal level. Equations 7-2 to 7-4 may be used to determine the power gain of an electronic circuit. In this case, the equations are correct only when the load resistance connected to the circuit output is equal to the circuit input resistance. However, it is common practice in the electronics industry to apply these equations regardless of the relationship between input and load resistances.

Frequency Response

Figure 7-7 shows a typical graph of amplifier output voltage or power plotted versus frequency. It is found that the output normally remains constant over a *middle range* of frequencies and falls off at low and high frequencies, due to the effects explained below. The gain over this middle range is termed the *mid-frequency gain*. The low frequency and high frequency at which the gain falls by 3 dB are designated f_1 and f_2, respectively. This range is normally considered the useful range of operating frequency for the amplifier, and the frequency difference $(f_2 - f_1)$ is termed the amplifier *bandwidth B*.

Frequencies f_1 and f_2 are sometimes termed the *half-power* or *3 dB points*. This is because, as shown in Example 7-4, the power output is −3 dB from its normal level when P_2 is half P_1. When the amplifier output is expressed as a voltage on the graph of frequency response, the 3 dB points (f_1 and f_2) occur when V_2 is 0.707 V_1. This relationship is shown in Example 7-5.

The falloff in amplifier gain at low frequency is due to the effect of coupling and bypass capacitors. Recall that the reactance of a capacitor is $X_c = 1/(2\pi fC)$. At medium and high frequencies, the factor f makes X_c very small, so that all coupling and bypass capacitors behave as short circuits. At low frequencies, X_c increases and some of the signal voltage is potentially divided across the capacitors [see Fig. 7-8(a)]. As the signal frequency gets lower, the capacitor reactances increase and the circuit gain continues to fall.

All transistors have capacitances between their terminals (Section 3-8). As shown in Fig. 7-8(b), there are also *stray capacitances* C_s, which are the capacitances between connecting wires and ground. All these capacitances are

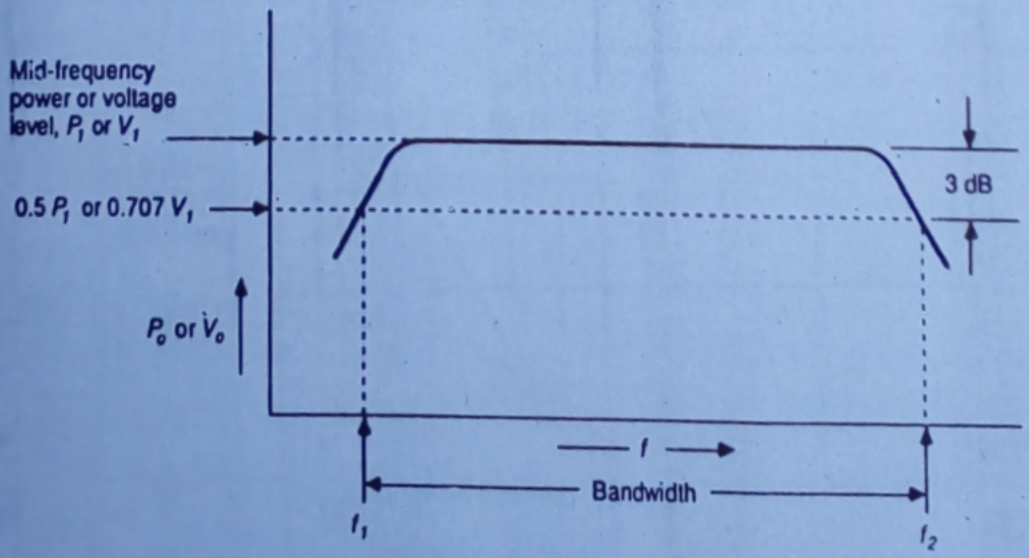
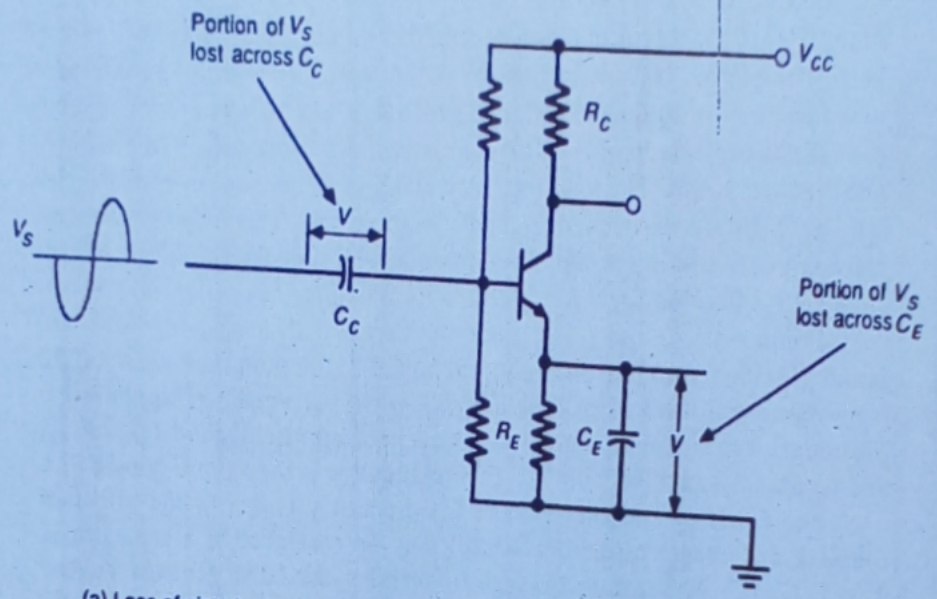
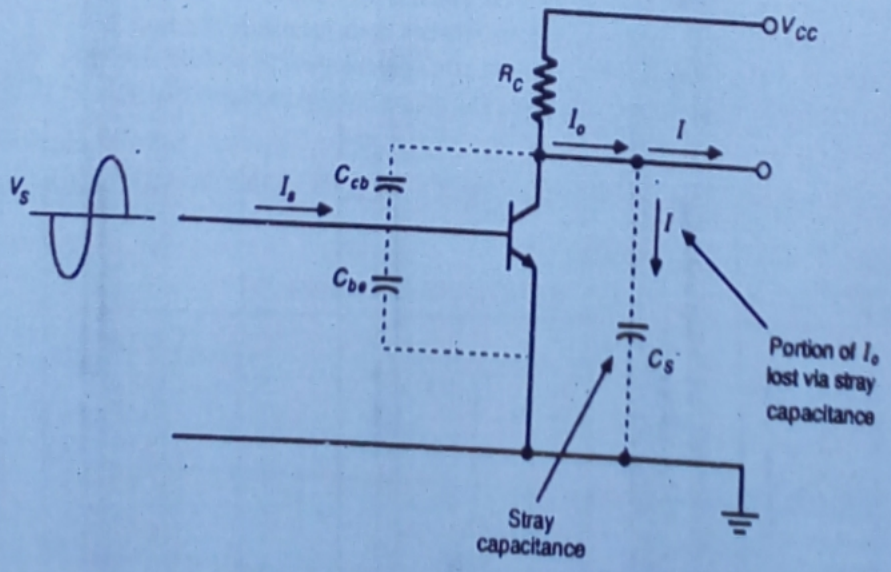


Figure 7-7 The output voltage (and output power) of an amplifier normally remains constant over a range of signal frequencies and falls off at high- and low-frequency extremes.



(a) Loss of signal voltage across coupling and bypass capacitors at low frequency



(b) Loss of output current via stray capacitance at high frequency

Figure 7-8 Low-frequency falloff in an amplifier output is normally due to loss of signal across capacitors. High-frequency falloff may be due to stray capacitance shunting output and input terminals.

very small, so that at low and medium frequencies their impedances are very high. As frequency increases, the reactances of the stray capacitances fall. When these reactances become small enough, they begin to shunt away some of the input and output currents and thus reduce the circuit gain. As the frequency gets higher and higher, the circuit gain continues to fall until it becomes too small to be useful. It can be shown that the upper 3-dB point for the amplifier can occur when the reactance of the stray capacitance is equal to the load resistance value.

Even if no external stray capacitances were present, the device internal capacitances and the *transit time* of charge carriers across the transistor junctions and through the semiconductor material limit the circuit frequency response. This limitation is expressed as a *cutoff frequency* f_α, which is the frequency at which the transistor current gain falls to 0.707 of its gain at low and medium frequencies. The cutoff frequency can be expressed in two ways, the *common emitter cutoff frequency* f_{α_e} or the *common base cutoff frequency* f_{α_b}. f_{α_e} is the frequency at which the common emitter current gain h_{fe} falls to 0.707 × (mid-frequency h_{fe}). f_{α_b} is the frequency at which the common base current gain h_{fb} falls to 0.707 × (mid-frequency h_{fb}). It can be shown that

$$f_{\alpha_b} \approx h_{fe} f_{\alpha_e} \tag{7-5}$$

For maximum bandwidth, the stray capacitance should be kept to a minimum. Also, f_α should be several times greater than the signal frequency f_s at which the reactance of the stray capacitance equals the amplifier load resistance.

Example 7-6 A transistor with $f_{\alpha_b} = 5$ MHz and $h_{fe} = 50$ is employed in a common emitter amplifier. A 100 pF capacitor C_s is connected across the output terminals. Determine the upper 3 dB point (a) when $R_C = 10$ kΩ, and (b) when $R_C = 100$ kΩ. Assume that $R_L \gg R_C$.

Solution

(a) $R_C = 10$ kΩ. From Eq. 7-5,

$$f_{\alpha_b} \approx h_{fe} f_{\alpha_e}$$

$$f_{\alpha_e} \approx \frac{f_{\alpha_b}}{h_{fe}} = \frac{5 \text{ MHz}}{50} = 100 \text{ kHz}$$

C_s reduces the amplifier gain by 3 dB when

$$\frac{1}{2\pi f_s C_s} = R_C = 10 \text{ k}\Omega$$

$$f_s = \frac{1}{2\pi C_s R_C} = \frac{1}{2\pi \times 100 \text{ pF} \times 10 \text{ k}\Omega} = 159 \text{ kHz}$$